Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.098”**

**.070”**

**7 6 5**

**1 2 3 4**

**1432X**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 1432X**

**APPROVED BY: DK DIE SIZE .070” X .098” DATE: 11/14/17**

**MFG: ANALOG DEVICES THICKNESS .022” P/N: OP42NBC**

**DG 10.1.2**

#### Rev B, 7/1